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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/663,719	09/17/2003	Steve Yang	MSS0006-US	2239

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EXAMINER	
NGUYEN, LINH V	

ART UNIT	PAPER NUMBER
2819	

DATE MAILED: 10/01/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/663,719	YANG ET AL.	
	Examiner	Art Unit	
	Linh V Nguyen	2819	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 September 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-16* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *17 September 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This office action is in response to application No. 10/663719 filed on 09/17/03. Claims 1 – 16 are pending on this application.

Continuing

2. An application in which the benefits of 60/412,792 filed on 09/24/02.

Specification

3. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

4. The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Claim Objections

5. In claim 8 there is no antecedent basis for the wording, "wherein said adder is used to add ". There is no reference to "adder" earlier in the claim either in the form of an implied as well as a literal description from which an earlier antecedent reference may be made. There is no clear recitation in the claim to avoid possible confusion as to what is actually claimed. The claim fail to particularly point out and distinctly claim the

subject matter that the applicant considers to be the invention here. Clarification is required.

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

7. Claims 1 – 4, 6, 9 – 12, 14, and 15 are rejected under 35 U.S.C. 102(b) as being anticipated by Hiller U.S. Patent No. 5,187,481.

Regarding claim 1, Fig. 2 of Hiller discloses an apparatus for converting an analog image signal (12) into a digital image signal (28), said apparatus comprising: a pseudo random binary sequence generator (16) for generating a digital dither signal (Col. 4 lines 62 – 64); a digital-to-analog converter (18) for converting said digital dither signal into an analog dither signal (Col. 4 lines 64 – 66); a summing device (20) for generating a dithered image signal (output of 20) in response to said analog dither signal and said analog image signal (Col. 4 lines 67 – 68); and an analog-to-digital converter (22) for converting said dithered image signal into said digital image signal (col. 5 lines 1 – 5).

Regarding claim 2, wherein said summing device (20) is used to add said analog image signal with said analog dither signal (Col. 4 lines 67 – 68).

Regarding claim 3, Fig. 1 of Hiller discloses an apparatus for converting an analog image signal (12) into a digital image signal (28), said apparatus comprising: a pseudo random binary sequence generator (16) for generating a digital dither signal (Col. 4 lines 62 – 64); a scrambler (multiply device 30 disclosing the digital data signal 28 and dither signal of 16 are mix together; wherein mix together is a definition of scrambler. See Webster Dictionary) for receiving an offset signal (digital data at 28 is input into 30) and generating a dithered offset signal (GAIN CONTROL; See Col. 5 lines 22 - 26) by scrambling said offset signal with said digital dither signal (Col. 5 lines 22 - 26); a digital-to-analog converter (18) for converting said dithered offset signal into an analog dithered offset signal (Col. 4 lines 64 - 66); a summing device (20) for generating a dithered image signal (output of 20) in response to said analog dithered offset signal (GAIN CONTROL) and said analog image signal (12); and an analog-to-digital converter (22) for converting said dithered image signal (output of 20) into said digital image signal (28).

Regarding claim 4, wherein said summing device (20) is used to add said analog image signal (12) with said analog dithered offset signal (output of 18. See Col. 67 – 68).

Regarding claim 6, Fig. 6 of Hiller discloses an apparatus for converting an analog image signal (12) into a digital image signal (28), said apparatus comprising: a

pseudo random binary sequence generator (16) for generating a digital dither signal (Col. 4 lines 62 – 64); an adder (82) for receiving an offset signal (output signal of 80) and generating a dithered offset signal (output signal of 82) by adding said offset signal with said digital dither signal (See Col. 10 lines 64 – 67); a digital-to-analog converter (18) for converting said dithered offset signal (output of 82) into an analog dithered offset signal (Col. 10 lines 67 – 68); a summing device (20) for generating a dithered image signal (output of 20) in response to said analog dithered offset signal (output of 18) and said analog image signal (12; See Col. 4 lines 67 – 68); and an analog-to-digital converter (44, 46) for converting said dithered image signal (output of 20) into said digital image signal (28, See Col. 5 lines 1 – 4).

Regarding claim 9, Fig. 2 of Hiller disclose a method for converting an analog image signal (12) into a digital image signal (18), said method comprising the following steps of: (a) generating a digital dither signal (Col. 4 lines 62 – 63); (b) converting (18) said digital dither signal into an analog dither signal (col. 4 lines 64 – 66); (c) adding (20) said analog image signal (12) with said analog dither signal (output of 18) to generate a dithered image signal (output of 20); and (Col. 4 lines 67 – 68); (d) converting (22) said dithered image signal into said digital image signal (Col. 5 lines 1 – 4).

Regarding claim 10, wherein said digital dither signal is provided with pseudo random binary sequence (Col. 4 lines 62 – 64).

Regarding claim 11, Fig. 1 of Hiller disclose a method for converting an analog image signal (12) into a digital image signal (28), said method comprising the following steps of: (a) generating a digital dither signal (Col. 4 lines 62 – 63); (b) scrambling (multiply device 30 disclosing the digital data signal 28 and dither signal of 16 are mix together; wherein mix together is a definition of scrambling. See Webster Dictionary) an offset signal (digital data at 28 is input into 30) with said digital dither signal (digital dither signal of 16 input into 30) to generate a dithered offset signal (GAIN CONTROL); (c) converting (18) said dithered offset signal into an analog dithered offset signal (Col. 4 lines 64 - 66); (d) adding (20) said analog image signal (12) with said analog dithered offset signal (output of 18) to generate a dithered image signal (output of 20); and (e) converting (22) said dithered image signal into said digital image signal (Col. 5 lines 1 – 4).

Regarding claim 12, wherein said digital dither signal is provided with pseudo random binary sequence (Col. 4 lines 62 – 64).

Regarding claim 14, Fig. 6 of Hiller disclose a method for converting an analog image signal (12) into a digital image signal (28), said method comprising the following steps of: (a) generating a digital dither signal (Col. 4 lines 62 – 63); (b) adding (82) an offset signal (output signal of 80) with said digital dither signal (output of 16) to generate a dithered offset signal (output of 82); (c) converting (18) said dithered offset signal into an analog dithered offset signal (Col. 10 lines 67 – 68); (d) adding (20) said analog

image signal (12) with said analog dithered offset signal (output of 18) to generate a dithered image signal (output of 20); and (e) converting (44, 46) said dithered image signal into said digital image signal (28).

Regarding claim 15, wherein said digital dither signal is provided with pseudo random binary sequence (Col. 4 lines 62 – 64).

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. Claims 5, 7, 8, 13, 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hiller as applied to claims 3, 11 and 14 above, and further in view of Brooks U.S. Patent No. 6,577,257.

Regarding claim 5, Fig. 1 of Hiller as applied to claim 3 above disclose the scrambler (30) is used to scramble (mix together. Webster Dictionary) the offset signal (digital data at 28 is input to 30) with said digital dither signal (digital dither signal of 16 input into 30). However, Hiller fails to disclose wherein said scramble at least one least significant bit of said offset signal.

Fig. 4 of Brooks discloses a system for digital dither having scrambler (102) use

to scramble (mix together. Webster Dictionary) the offset signal (106) with digital dither signal (Brooks, Col. 4 lines 34 – 36); wherein the said scramble at least one least significant bit of said offset signal (Brooks, Col. 7 lines 48 – 54; Also see Fig. 5 [504] for disclosing leas significant bit [LSB] BIT 0 of offset signal 106).

Hiller and Brooks are common subject matter of Analog-to-Digital converter with digital dither. Therefore it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporated the least-significant-bit of the offset signal taught by Brooks into scrambling of the offset signal of Hiller for the purpose of reduced quantization noise, increase dynamic range performance, and increase signal bandwidth (Brooks, Col. 4 lines 18 – 20).

Regarding claim 7, Fig. 1 of Hiller modified by Brooks as applied to claim 5 above, further discloses wherein said summing device (Hiller, Fig.1 [20]) is used to add said analog image signal (Hiller, Fig. 1 [12]) with said analog dithered offset signal (Hiller, Fig. 1 [output of 18]).

Regarding claim 8, Fig. 1 of Hiller modified by Brooks as applied to claim 5 above, disclosed the scrambler (Hiller, Fig.1 [30]) to scramble (mix together. Webster Dictionary) at least one least significant bit of said offset signal with the digital dither signal. However, Hiller's Fig. 1[30] does not disclose an adder is used to add the at least one least significant bit of the offset signal with the digital dither signal.

Fig. 4 of Brooks incorporated into Hiller as applied to claim 5 above, further

discloses Brook's [102] is an adder (Brooks, Col. 4 lines 34 – 36) to add at least one of least significant bit of the offset signal with the digital dither signal.

Hiller and Brooks are common subject matter of Analog-to-Digital converter with digital dither. Therefore it would have been obvious to one having ordinary skill in the art at the time the invention was made to modified the scrambling device of Hiller (Fig. 1[30]) with the adding device taught by Brooks (Fig. 4 [102]; Col. 4 lines 34 – 36) for the purpose of reduced quantization noise, increase dynamic range performance, and increase signal bandwidth (Brooks, Col. 4 lines 18 – 20).

Regarding claim 13, Fig. 1 of Hiller as applied to claim 11 above disclosed scrambling (multiply device 30 disclosing the digital data signal 28 and dither signal of 16 are mix together; wherein mix together is a definition of scrambling. See Webster Dictionary) an offset signal (digital data at 28 is input into 30) with said digital dither signal (digital dither signal of 16 input into 30) to generate a dithered offset signal (GAIN CONTROL). However, Hiller fails to disclose wherein at least one least significant bit of said offset signal is scrambled with said digital dither signal.

Fig. 4 of Brooks discloses a system for digital dither having: scrambling (102, mix together. Webster Dictionary) at least one least significant bit (Brooks, Col. 7 lines 48 – 54; Also see Fig. 5 [504] for disclosing leas significant bit [LSB] BIT 0) of the offset signal (106) with digital dither signal (Brooks, Col. 4 lines 34 – 36).

Hiller and Brooks are common subject matter of Analog-to-Digital converter with digital dither. Therefore it would have been obvious to one having ordinary skill in the art

at the time the invention was made to incorporated the least-significant-bit of the offset signal taught by Brooks into scrambling of the offset signal of Hiller for the purpose of reduced quantization noise, increase dynamic range performance, and increase signal bandwidth (Brooks, Col. 4 lines 18 – 20).

Regarding claim 16, Fig. 6 of Hiller as applied to claim 14 above disclosed adding (82) an offset signal (output signal of 80) with said digital dither signal (output of 16) to generate a dithered offset signal (output of 82). However, Hiller fails to disclose wherein at least one least significant bit of said offset signal is added with said digital dither signal.

Fig. 4 of Brooks discloses a system for digital dither having: adding (102, (Brooks, Col. 4 lines 34 – 36) at least one least significant bit (Brooks, Col. 7 lines 48 – 54; Also see Fig. 5 [504] for disclosing leas significant bit [LSB] BIT 0) of the offset signal (Brooks, Fig. 4 [106]) with digital dither signal (Brooks, Col. 4 lines 34 – 36).

Hiller and Brooks are common subject matter of Analog-to-Digital converter with digital dither. Therefore it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporated the least-significant-bit of the offset signal taught by Brooks into the offset signal of Hiller for the purpose of reduced quantization noise, increase dynamic range performance, and increase signal bandwidth (Brooks, Col. 4 lines 18 – 20).

Cited References

10. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. The cited references relate to Analog to Digital converter with dither digital signal.

Contact Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Linh Van Nguyen whose telephone number is (571) 272-1810. The examiner can normally be reached from 8:30 – 5:00 Monday-Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mr. Michael Tokar can be reached at (571) 272-1812. The fax phone numbers for the organization where this application or proceeding is assigned are (703-872-9306) for regular communications and (703-872-9306) for After Final communications.

09/22/2004

Linh Van Nguyen 

Art Unit 2819